INTEGRATED, STEP-DOWN SWITCHING REGULATOR WITH CCM OPERATION

Device Type	Current Rating	Input Voltage	Output Voltage
VT261	20A (CCM)	6.5V to 14.0V	0.7V to 5.5V

GENERAL DESCRIPTION

The VT261 is a member of Maxim's fifth generation of fully-integrated, highly efficient switching regulators for applications operating from 6.5V to 14.0V and requiring up to 20A maximum load. This single-chip regulator provides an extremely compact, fast and accurate power delivery solution for low-output voltage applications. The VT261 Continuous Current Mode (CCM) operation down to light load provides best possible load regulation, ripple and output voltage headroom performance. Two internal low dropout (LDO) regulators power the IC analog (A_{VDD}), logic and gate drive sections (V_{CC}). The proprietary architecture maintains tight voltage regulation in both modes.

This regulator allows designers to program soft start and switching frequency/inductor ripple current. The programmable features can be used to make trade-offs between the voltage regulators' performance and cost.

KEY FEATURES

- Small Footprint
- Low-Profile Solution: 1.4mm to 4mm Maximum Height
- High-Efficiency Solution: Greater Than 95% Peak Efficiency
- CCM Operation
- Fast Transient Response: Supports up to 300A/µs Load Step Transients
- Minimum Input and Output Capacitance Using Only MLCC Capacitors
- No External Frequency Compensation Required.
- High-Frequency Operation: Greater Than 1MHz

ADDITIONAL FEATURES

- Two AC Droop Options
- Two I_{MAX} Options
- Supports Differential Remote Sense
- Programmable Soft Start
- Cycle-by-Cycle Current Limiting
- Output Short Circuit Protection
- Undervoltage and Overvoltage Lockout
- Power Good Indicator
- Thermal Shutdown
- Programmable Peak-to-Peak Current Ripple
- Internal 3.3V LDO Analog Supplies A_{VDD}
- Internal 3.3V LDO Logic and Gate Drive Supply V_{CC}

APPLICATIONS

- DC-DC Converters Modules and On-Board, Point-of-Load Voltage Regulators
- Networking and Communication Equipment
- Storage, Servers and Workstations
- Industrial Equipment

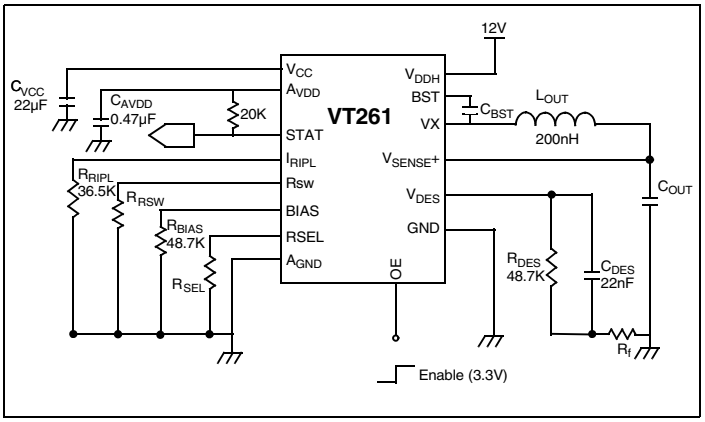


Figure 1: Basic Application Circuit

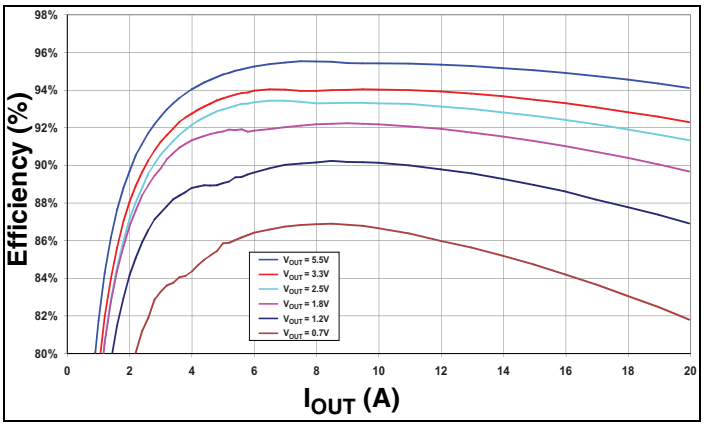


Figure 2: VT261 System Efficiency vs. Output Load

Ordering Information

Part Number	Current Level	Package	Drawing Number	Shipping Method	Package Marking
RoHS Compliant[3]					
VT261WFQR-ADJ	20A	QFN-16 [Type C]	ES AP-2104	250u Tape & Reel	VT261WF
VT261WFQX-ADJ				2.5ku Tape & Reel	

ABSOLUTE MAXIMUM RATING[1]

VSENSE+, OE, R_SEL, VCC, AVDD, Rsw, I_{RIPL}, BIAS, V_{DES} and STAT Pin Voltages (3.3V) .....-0.3V to 4V

Input Pin Voltages(V_{DDH}) DC.....-0.3V to 16V

Switching Node Voltage (VX) DC.....-0.3V to 16V

Switching Node Voltage (VX) 25ns[2] .....-10V to 23V

V_{DDH} Pin - VX Pin Differential 25ns[4] .....-10V to 23V

V_{DDH} Pin 25ns .....-0.3V to 19V

BST Pin (BST) DC .....-0.3V to 20V

BST Pin (BST) 25ns.....-6.0V to 27V

BST Pin - VX Pin Differential..... 4V

Junction Temperature (T_J).....150°C

Storage Temperature Range..... -65°C to 150°C

Peak Reflow Temperature Lead-Free .....260°C

OPERATING RATINGS

Input Voltage (V_{DDH}).....6.5V to 14V

Junction Temperature (T_J) ..... -40°C to 125°C

Output Current (I_{OUT})..... 20A

THERMAL RATINGS

Θ_{JC} Max..... 0.57°C/W

Θ_{JA} Typ[5] (Still Air, No Heatsink)..... 16°C/W

Note 1: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The 25ns rating is the allowable voltage that the VX node may exceed the -0.3V to 16V ratings in either positive or negative direction for up to 25ns per cycle.

Note 3: These products are completely Halogen-free and Pb-free, employing special materials sets: molding compounds/die attach materials and 100% matte tin plate including anneal. These products are RoHS compliant with an -e3 termination finish and are compatible with both SnPb and Pb-free soldering operations. These products are MSL classified at peak reflow temperatures that meet JEDEC JSTD-020.

Note 4: The V_{DDH} input pin voltage AC should not exceed 19V (25ns). This measurement is taken at the V_{DDH} pin referenced to V_{SS} pin immediately adjacent using a high frequency scope probe with I_{LOAD} at I_{MAX}. A high-frequency input bypass capacitor must be located less than 60mils from the V_{DDH} pin and the Maxim device per our design guidelines.

Note 5: Data taken using Maxim's evaluation kit.

Electrical Characteristics

V_{DDH} = 12V±10%, unless otherwise specified. The ✻ denotes specifications which apply over the full operating junction temperature range (T_J = -40 to 125°C). Otherwise, specifications are for T_J = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
Supply Voltage (V_{DDH})							
V_{DDH}	Input Voltage Range		✻	6.5		14	V
$I_{DD, SHUTDOWN}$	Input DC Supply Current, Shutdown	OE = LOW				1	µA
V_{CC}	Internal Gate Drive Supply Voltage	OE = HIGH		2.97	3.3	3.63	V
A_{VDD}	Internal Analog Supply Voltage	OE = HIGH		2.97	3.3	3.63	V
Output Voltage[1]							
V_{OUT}	Output Voltage Range		✻	0.7		5.5	V
–	Timing OE HIGH to V_{OUT} Rise	OE HIGH, No Soft Start	✻		300		µs
Reference Voltage							
V_{DES0}	Reference Voltage	R_{DES} = R_{BIAS} = 48.7kΩ, Tolerance 0%, T_J = 0 to 100°C			1.21		
	V_{DES} Accuracy			-0.5		+0.5	%
V_{DES}	Voltage Range		✻	0.7		1.8	V
V_{SENSE+}	Voltage Range		✻	0.7		1.8	V
Error Amplifier							
V_{IN-OS}	Input Offset Voltage		✻			±2	mV
τ	Integrator Time Constant			6.4	10	14.4	µs
Maximum Current (Average)							
I_{MAX}	Maximum DC Load Current	R_SEL = 0Ω or 11kΩ	✻	20			A
		R_SEL = 22kΩ or 91kΩ	✻	13.3			A
Current Limit - Load (Average)							
–	Load Current Limit Inception	I_{MAX} = 20A		22	27	31	A
	Load Current Limit Continuous			20	25	28	A
	Load Current Limit Inception	I_{MAX} = 13.3A		15	18	21	A
	Load Current Limit Continuous			13	17	19	A
Undervoltage Lockout (V_{DDH})							
$FUVLO_{UPPER}$	Undervoltage Lockout Upper Threshold		✻	5.8	6.2	6.5	V
$FUVLO_{LOWER}$	Undervoltage Lockout Lower Threshold		✻	5.2	5.6	6.0	V
Undervoltage Lockout (A_{VDD})							
$AUVLO_{UPPER}$	A_{VDD} Undervoltage Lockout Upper Threshold		✻	2.69	2.85	3.00	V
$AUVLO_{LOWER}$	A_{VDD} Undervoltage Lockout Lower Threshold		✻	2.60	2.76	2.90	V
Overvoltage Lockout (V_{DDH})							
$FOVLO_{UPPER}$	V_{DDH} Overvoltage Lockout Upper Threshold		✻	14.4	14.68	15.2	V
R_SEL Pin							
–	Maximum Voltage					3.63	V
Status							
$V_{OL-STAT}$	Status Output Low Voltage	I_{OUT} = 4mA				0.4	V
$I_{OL-STAT}$	Status Current Sink Capability	V_{OUT} = 0.4V		15	25		mA
$I_{OH-STAT}$	Status Output High Leakage Current		✻			500	nA

Note 1: It is required that (V_{DDH} - V_{OUT}) > 2V.

Note 2: VIH should not exceed A_{VDD} + 0.3V.

Electrical Characteristics

V_{DDH} = 12V±10%, unless otherwise specified. The ∗ denotes specifications which apply over the full operating junction temperature range (T_J = -40 to 125°C). Otherwise, specifications are for T_J = 25°C.

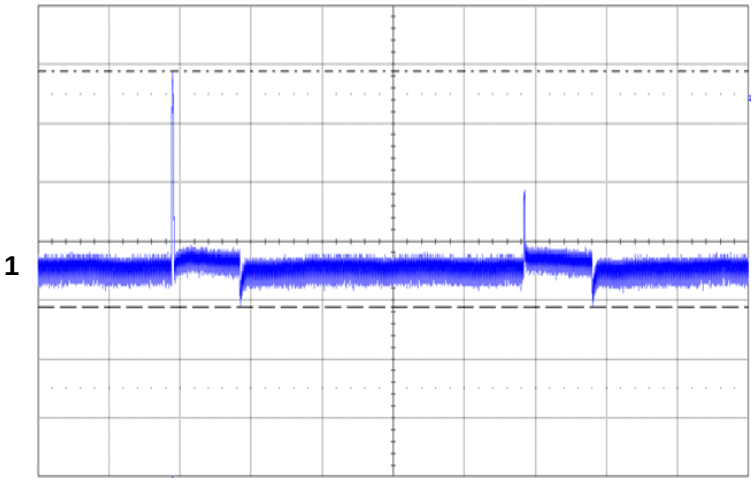
Symbol	Parameter	Conditions			Min	Typ	Max	Units
Output Enable								
V_{IH}	Input High Voltage[2]				2.2			V
V_{ILOE}	Input Low Voltage						0.8	V
I_{IN-LLH}	Input Current - Logic Level HIGH						10	µA
BIAS Pin								
V_{BIAS}	Voltage on BIAS Pin					1.21		V
I_{RIPL} Pin								
V_{IRIPL}	Voltage On I_{RIPL} Pin					1.21		V
I_{IRIPL}	Pin Current Range	Programmable with R_{RIPL} Resistor			20		100	µA
Rsw Pin								
V_{Rsw}	Voltage on Rsw Pin					1.21		V
I_{RSW}	Pin Current Range	Programmable with Rsw Resistor			20		100	µA
Switching Current Amplifier								
Ki	Current Gain Setting (I_{OUT}/I_{ERROR})	R_{SEL} = 0Ω or 91kΩ				400,000		
		R_{SEL} = 11kΩ				133,000		
		R_{SEL} = 22kΩ				267,000		
Power Good (PWRGD)								
$V_{TH-UPPER}$ (CCM)	Fault Assertion Threshold	V_{OUT} Below V_{DES} as %			5.7	8.3	10.9	%
$V_{TH-LOWER}$ (CCM)	Fault Recovery Threshold				4.4	6.7	9	%
–	Deglitch Delay Time				25		35	µs
–	Power Good Blanking Time On Startup				3.2		4.5	ms
Overvoltage Protection (OVP)								
$V_{TH-UPPER}$ (CCM)	Fault Assertion Threshold	V_{OUT} Above V_{DES} as %			5.7	8.3	10.9	%
$V_{TH-LOWER}$ (CCM)	Fault Recovery Threshold				4.4	6.7	9	%
–	Deglitch Delay Time				25		35	µs
Thermal Shutdown (Specified by Design)								
T_{SHDN}	Shutdown				140	150	160	°C
	Shutdown Hysteresis					23		°C
Regulation and System Specifications (Specified by Design, tested using circuit in Figure 9)								
–	Line Regulation	I_{OUT} = 20A			-2		2	mV
–	Load Regulation	RFB1 = 0			-2		2	mV
–	Output Voltage Accuracy	V_{OUT} = 1.2V, Using R_{BIAS} and R_{DES} 0.5% Tolerance Resistors, Worst Case.		∗	-2.2		2.2	%
Eff	Peak Efficiency	F_{SW} = 600kHz I_{OUT} = 7A V_{DDH} = 12V	V_{OUT} = 1.2V			90.2		%
			V_{OUT} = 3.3V			94.0		%
	TDP Efficiency (2/3 of I_{max})	F_{SW} = 600kHz I_{OUT} = 13A V_{DDH} = 12V	V_{OUT} = 1.2V			89.5		%
			V_{OUT} = 3.3V			93.9		%

Note 1: It is required that (V_{DDH} - V_{OUT}) > 2V.

Note 2: VIH should not exceed A_{VDD} + 0.3V.

Typical Operating Characteristics

Transient Response

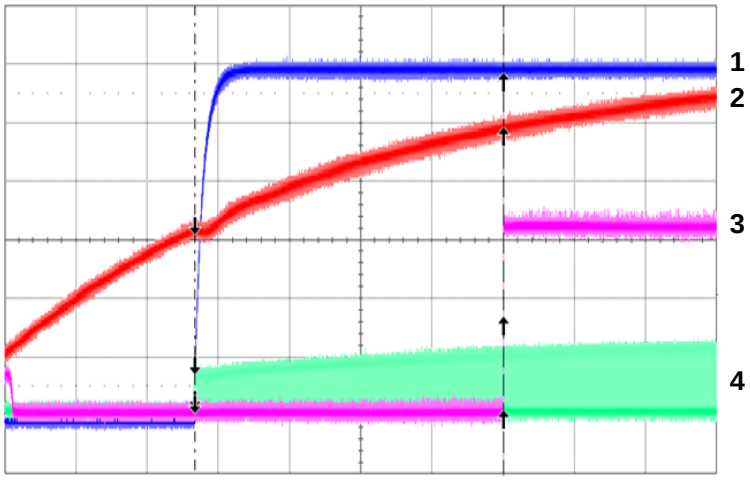


Time/Div: 20µs

Conditions: V_{IN} = 12V
V_{OUT} = 1.2V
I_{OUT} = 0-20A Step
Slew = 300A/µS
C_{OUT} = 14 x 22µF
L_{OUT} = 210nH

1. V_{OUT} (50mV/div)

Startup Response

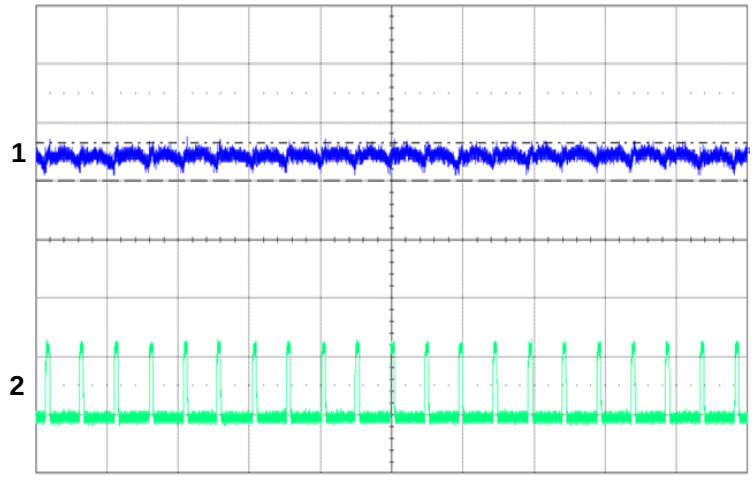


Time/Div: 1.0ms

Conditions: V_{IN} = 12V
V_{OUT} = 1.2V
I_{OUT} = 20A
C_{OUT} = 14 x 22µF
L_{OUT} = 210nH

1. V_{OUT} (200mV/div)
2. V_{IN} (2V/div)
3. STAT (1V/div)
4. VX (10V/div)

Typical V_{OUT} Ripple

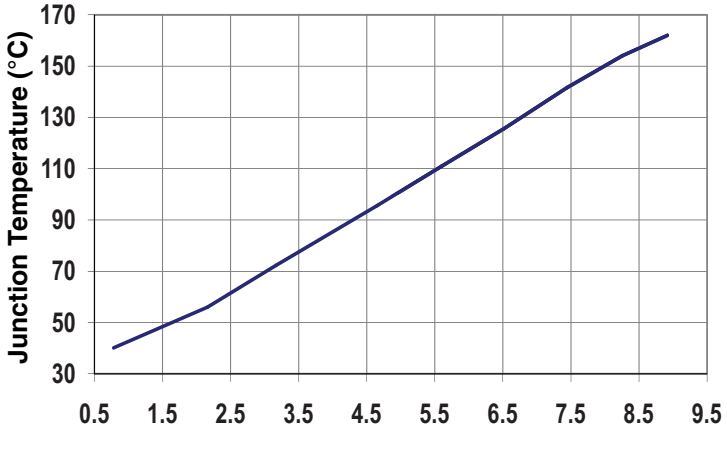


Time/Div: 2µs

Conditions: V_{IN} = 12V
V_{OUT} = 1.2V
Fsw = 1MHz
I_{OUT} = 20A
C_{OUT} = 14 x 22µF
L_{OUT} = 210nH

1. V_{OUT} (20mV/div)
2. VX (10V/div)

Junction Temperature vs Power Dissipation

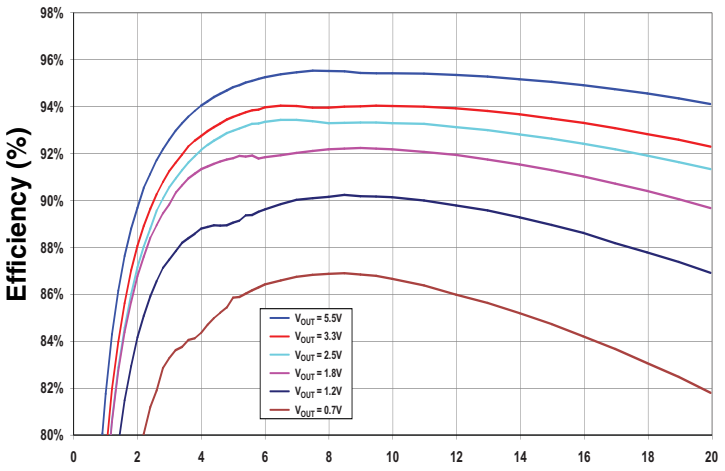


Power Dissipation (W)

Conditions: V_{IN} = 12V
Fsw = 450 - 650kHz
T_A = 25°C
C_{OUT} = 14 x 22µF
L_{OUT} = 210nH

Typical Operating Characteristics

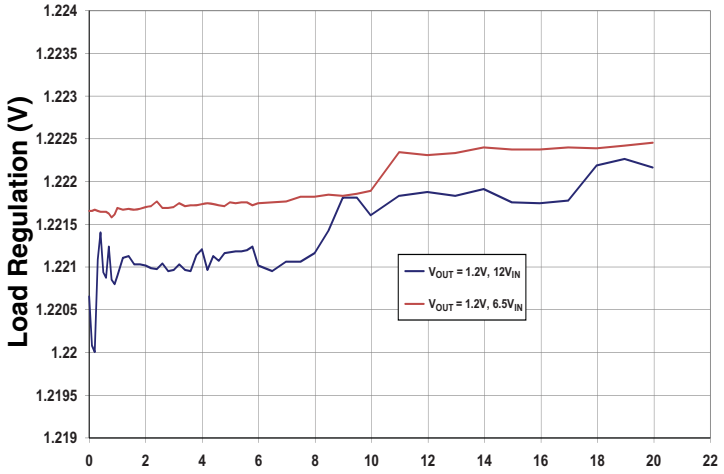
System Efficiency vs. Output Load



I_{OUT} (A)

Conditions: V_{IN} = 12V
Fsw = 450 - 800kHz
T_A = 25°C
C_{OUT} = 14 x 22µF
L_{OUT} = 210nH

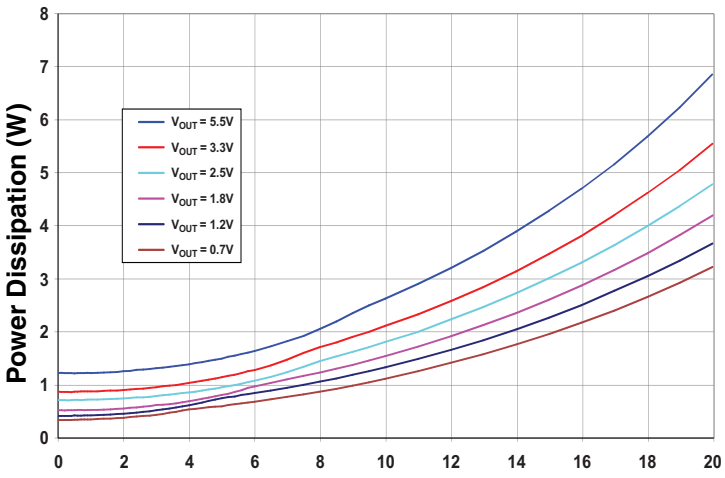
Load Regulation



I_{OUT} (A)

Conditions: Fsw = 550kHz
T_A = 25°C
L_{OUT} = 210nH

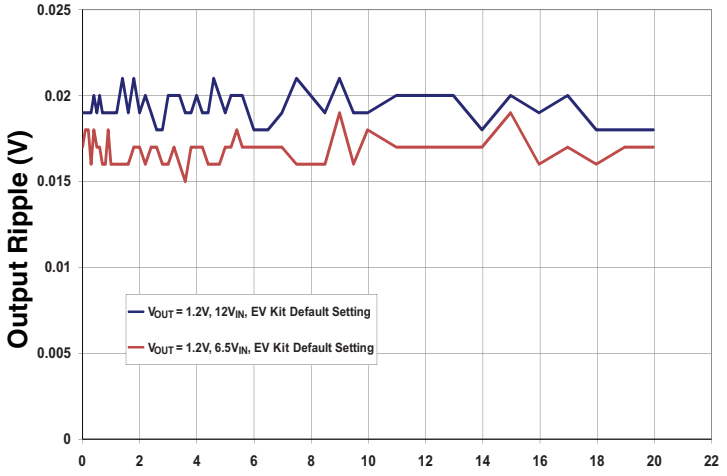
System Power Dissipation



I_{OUT} (A)

Conditions: V_{IN} = 12V
Fsw = 450 - 800kHz
T_A = 25°C
L_{OUT} = 210nH

Output Ripple

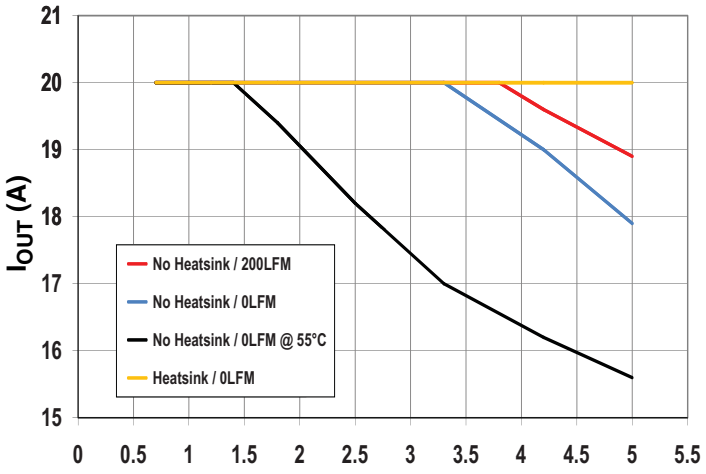


I_{OUT} (A)

Conditions: Fsw = 550kHz
T_A = 25°C
L_{OUT} = 210nH

Typical Operating Characteristics

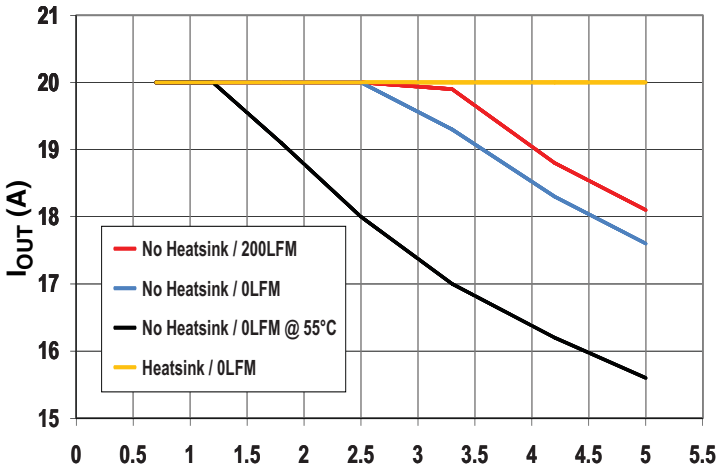
Safe Operating Area (SOA)



V_{OUT} (V)

Conditions: V_{IN} = 12V
Fsw = 450 - 650kHz
T_A = 25°C
L_{OUT} = 210nH

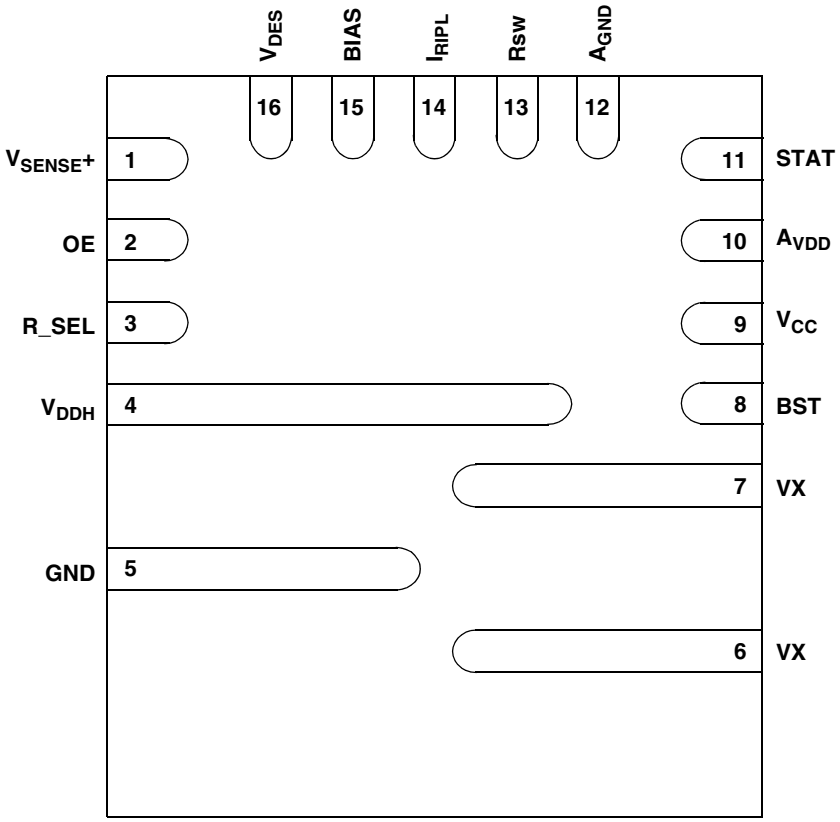
Safe Operating Area (SOA)



V_{OUT} (V)

Conditions: V_{IN} = 6.5V
Fsw = 450 - 650kHz
T_A = 25°C
L_{OUT} = 210nH

Pinout and Block Diagrams



(TOP VIEW)

Figure 3: VT261 Pinout (QFN-16)

CONNECTION INFORMATION

V_{SENSE}+ (Pin 1): Output voltage feedback node. A resistor divider could be used to regulate the output above its reference voltage.

OE (Pin 2): Output enable node. When the voltage at this node is HIGH, the voltage regulator is functioning. When it is LOW, the entire voltage regulator is shut down (including the LDOs). This node is internally-pulled LOW by a 400k resistor to GND.

R_SEL (Pin 3): System Configuration Resistor. This programming connection is used to configure the system at startup.

V_{DDH} (Pin 4): Input supply voltage node. This node connects to the input 12V power supply source.

GND (Pin 5): Internal Power FET Ground node. This node connects directly to the ground plane.

VX (Pins 6-7): Power FET Switching node. These nodes connect the switching node of the power devices to the output inductor.

BST (Pin 8): Bootstrap for high-side switch.

V_{CC} (Pin 9): Driver power supply voltage. Internal 3.3V.

A_{VDD} (Pin 10): Analog power supply voltage. Internal 3.3V.

STAT (Pin 11): Status node. When the voltage at this node is HIGH, the voltage regulator is functioning within normal operating parameters. This is an open-drain output and must be pulled up to A_{VDD}.

A_{GND} (Pin 12): Analog power ground node.

Rsw (Pin 13): Switching frequency selection resistor.

I_{RIPL} (Pin 14): A resistor from this node to A_{GND} is used to set the default indicator ripple current.

BIAS (Pin 15): Internal BIAS generator. This node buffers the internal accurate bandgap reference voltage. An accurate resistor of ±0.5%, 48.7k should be connected to this node.

V_{DES} (Pin 16): An accurate reference resistor and soft start capacitor are placed between this node and the remote sense ground to establish V_{OUT}.

OPERATION

The VT261 provides a highly integrated, compact solution for high efficiency, low voltage power conversion. The following sections describe, in detail, the use and operation of these regulators.

Control Architecture

A simplified block diagram is shown in Figure 5. This regulator family implements a true average current mode control algorithm that achieves stable switching operation without the need for external compensation. A description of the basic control loop follows. Voltage regulation is achieved by monitoring the difference between the desired output voltage on the V_{DES} pin and the actual output voltage across the load (V_{OUT}). The error amplier is connected as a voltage follower that tries to maintain its negative feedback terminal pin at the same voltage as the V_{DES} pin. Any difference in voltage between V_{SENSE}+ and V_{DES} causes an error current to flow through the internal resistor R_{FB}. This error current (I_{ERROR}) is sensed in the error amplier and fed to the Switching Current Amplier block.

The Switching Current Amplier block accepts three inputs: the error current signal (I_{ERROR}), the desired ripple current (I_{RIPL}) and the desired maximum current. The output of this block is a triangular waveform (shown in Figure 4), which appears at VX as the inductor output current I_{OUT}.

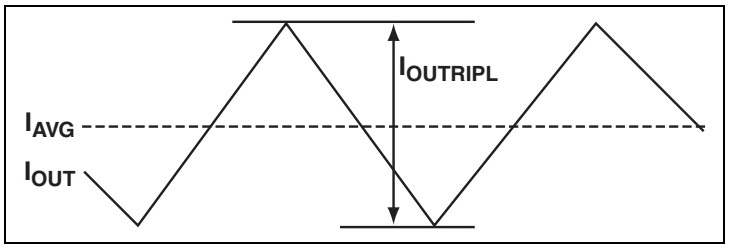


Figure 4: Inductor Ripple Current

The average value of this waveform (I_{AVG}) equals the I_{ERROR} amplied by a large gain factor (Ki). The average output current adjusts the output voltage in the appropriate direction to maintain regulation. Using proprietary on-chip current sensing, the Switching Current Amplifier block also maintains a constant peak-to-peak current amplitude (equal to $I_{OUTRIPL}$) that is independent of duty cycle, inductor value, input voltage or output voltage.

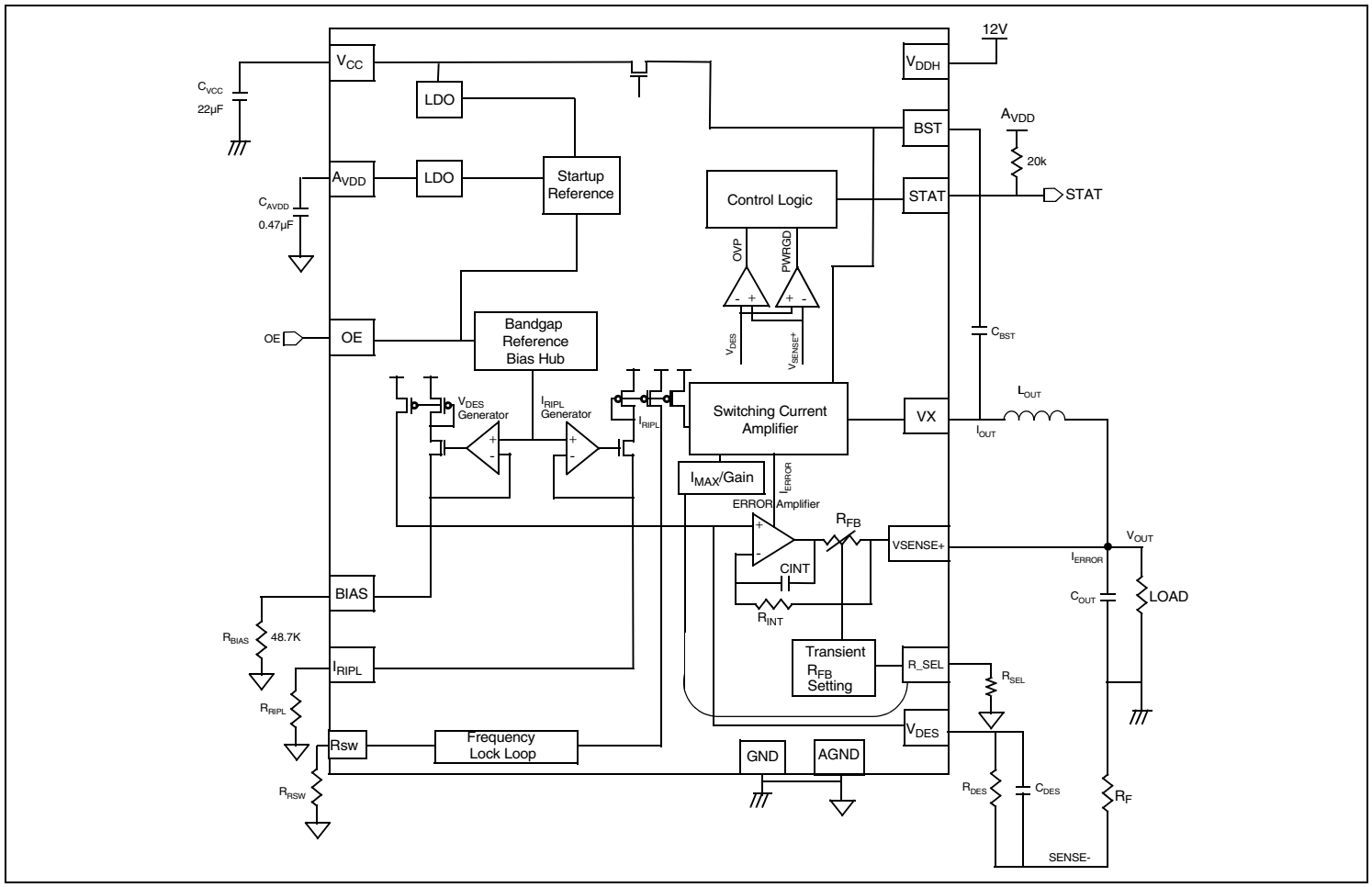


Figure 5: Functional Block Diagram

Operation

The voltage reference circuits support output regulation above or below the reference level (V_{DES0}). Initially, a reference bias current is established by forcing the bandgap voltage at the BIAS pin across the external resistor R_{BIAS}. The R_{BIAS} resistor MUST be 48.7k (±0.5%) to create the proper bias current reference for on chip circuitry. This bias current is mirrored and applied to the external resistor R_{DES} connected to the V_{DES} pin, resulting in a voltage at V_{DES} given by Equation 1:

Equation 1

$$V_{DES} = V_{DES0} \bullet \left(\frac{R_{DES} + R_F}{48.7k\Omega}\right)$$

V_{DES} is generated relative to the load ground, eliminating any error caused by differences in ground potential between the regulator and its load. Resistor tolerances for R_{DES} and R_{BIAS} directly affect the DC accuracy of the output voltage. Therefore, 0.1% resistors are recommended for high accuracy applications. It is also important to ensure that any resistance in the negative sense line is small compared to the value of R_{DES}. V_{DES} is restricted to be no lower than 0.7V and no greater than 1.8V. R_F is used for filtering the ground noise back to the error amplifier (560Ω recommended).

The Power Good and OVP comparators sense V_{SENSE}+ relative to V_{DES} to determine whether the output voltage is within regulator tolerance limits.

Error Amplifier Operation

The error amplier senses the error signal as a current rather than a voltage and is therefore implemented as a unity gain amplier with a capacitor C_{INT} for high-frequency feedback and a resistor R_{INT} to V_{SENSE}+ for DC feedback, as shown in Figure 6. The I_{ERROR} and regulator output current (I_{OUT}) have a fixed gain relationship set by the programmed value of Ki. The DC sensing at the V_{SENSE}+ pin forces the droop developed by $I_{ERROR} \bullet R_{FB}$ to be integrated away with a time constant of $R_{INT} \bullet C_{INT}$.

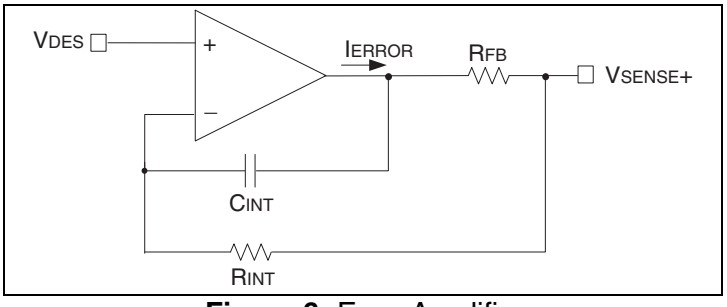


Figure 6: Error Amplifier

A transient voltage error will exist on V_{SENSE}+ during a load transient due to the high frequency gain set by the choice of R_FB. The magnitude of the transient voltage error on V_{SENSE}+ can be estimated by Equation 2:

Equation 2

$$V_{SENSE+ERROR} = I_{LOADTRANSIENT} \bullet \left(\frac{R_{FB}}{Ki}\right)$$

For example, a 10A load step on a VT261 with: Ki = 400,000, and R_{FB} = 600, a transient voltage error of approximately 15mV will be generated that will integrate away with a 10µs time constant.

Switching Frequency and Ripple Current Selection

The VT261 uses a frequency locked loop to set the switching frequency. The frequency can be programmed by selecting R_{RSW} according to Equation 3.

Equation 3

$$R_{RSW} = \frac{1}{F_{SW} \times k}$$

where F_{SW} = Switching Frequency

$k = 30 \times 10^{-12}$

The switching frequency can be programmed in the range of 500kHz to 1.5MHz.

The peak-to-peak output ripple current will be automatically adjusted to the programmed Fsw according to Equation 4:

Equation 4

$$F_{SW} = \frac{V_{OUT} \bullet (V_{IN} - V_{OUT})}{V_{IN} \bullet L_{OUT} \bullet I_{OUTRIPL}}$$

A second programming resistor R_{RIPL} is selected according to Equation 5.

Equation 5

$$R_{RIPL} = \frac{V_{IRIPL}}{I_{RIPL}}$$

$$I_{OUTRIPLDEFAULT} = I_{RIPL} \bullet 200000 + \frac{V_{DDH} - V_{OUT}}{L_{OUT}} \bullet 30ns + \frac{V_{OUT}}{L_{OUT}} \bullet 35ns$$

This programming resistor is required in order to provide a default setting of the output ripple current and reduce the time for frequency locking to the programmed value.

If R_{RSW} is tied to A_{VDD}, the frequency locked loop will be deactivated and the output ripple current will be programmed by R_{RIPL} alone.

Operation

Minimum ON-Time Consideration

The high and low-side switches have a minimum ON time of approximately 100ns, which limits the maximum frequency that can be programmed. The application must ensure operation with pulse width that is higher than this minimum ON time. This is necessary for the circuit to operate without a filter, which can cause high output ripple. In any application, the condition in Equation 6 must be satisfied.

Equation 6

$$Fsw \leq \frac{V_{OUT}}{V_{IN} \times t_{ON(min)}}$$

For example, if V_{OUT} = 0.9V and V_{IN} = 12V, then Fsw $\leq$ 750kHz.

Voltage Regulator Enable

The output enable (OE) signal enables/disables the regulator and its internal LDOs. OE must be driven by and external 3.3V logic signal. OE signal HIGH enables the regulator to switch. A logic level LOW disables switching and turns off static current on the regulator. This signal is internally pulled LOW and has TTL compatible threshold levels. The regulator has a soft shutdown feature that ramps the switching current down to zero before turning off the internal FETs. This applies to all shutdown behaviors due to OE-off and soft faults. Once OE is HIGH, there is a delay of 300µs to decode the R_SEL settings and charge C_{BOOST} by turning on the low-side switch prior to V_{OUT} startup.

Soft Start

Regulator startup is governed by the choice of the C_{DES} capacitor, which sets the rise time of the reference voltage generated on the V_{DES} pin, according to R_{DES} x C_{DES} time constant. C_{DES} also improves high-frequency sensing of the load ground. A minimum recommended value of C_{DES} is 1000pF. The Power Good and OVP comparators are masked out for 4ms after the regulator is enabled, during which time the V_{DES} voltage is expected to settle within the Power Good threshold. Therefore, the soft start time constant is recommended to be no greater than 1ms.

FUVLO and FOVLO Protection

The regulator internally monitors V_{DDH} with both Undervoltage Lockout (UVLO) and Overvoltage Lockout (OVLO) circuits. When the input supply voltage is below the UVLO thresholds or above the OVLO thresholds, the regulator stops switching, and the STAT pin is driven LOW. For UVLO and OVLO levels, refer to the Electrical Characteristics table.

Overtemperature Protection

If the die temperature reaches approximately 150°C during operation, a temperature-sensing circuit disables the regulator and the STAT pin is driven LOW. Once the temperature falls below 127°C, the regulator will re-enable itself.

Current Limiting and Short Circuit Protection

The regulator's current mode control architecture provides inherent cycle-by-cycle current limiting and short circuit protection. Instantaneous peak currents are monitored and controlled on a cycle-by-cycle basis within the Switching Current Amplifier block and are limited to the average current limit plus one half the output ripple current.

The average current limit value is defined in the Electrical Characteristics table.

AUVLO Protection

The regulator internally monitors A_{VDD} for undervoltage lockout (UVLO). When the input supply voltage is below the UVLO threshold, the regulator stops switching, and the STAT pin is driven LOW. For UVLO levels, refer to the Electrical Characteristics table. When AUVLO protection is activated, the regulator will turn off immediately without a soft shutdown. Please reference the Regulator Status section for details on STAT behavior.

Power Good Detection

Power Good detection covers both UVP and OVP. An internal overvoltage and power good detection comparator is used to detect when the output voltage is within the specified tolerance limit. Referring to Figure 5, the comparator monitors the difference between V_{DES} and V_{SENSE}+ for both overvoltage (OVP) and undervoltage (UVP) conditions.

The PWRGD threshold levels are set to a fixed 8.3% above and below the V_{DES} voltage. The PWRGD detection circuit is filtered by a 30µs deglitch filter to allow for brief transient excursions beyond the present threshold levels. The Power Good status is reported on the STAT pin.

For more detail on the PWRGD tolerances, refer to the Electrical Characteristics table.

Voltage Margining

Voltage margining can be achieved by changing the effective resistance of R_{DES}. R_{DES} can be changed by using external switches or FETs driven by TTL signals in order to introduce parallel resistors to decrease the effective value of R_{DES}.

Regulator Status

When OE is HIGH, the regulator status (STAT) signal provides an open-drain output, consistent with CMOS logic levels, that indicates whether the regulator is functioning properly. It should be externally-pulled HIGH (using a pull-up resistor) during normal device operation, and is driven LOW when one or more of the following conditions exist:

- The regulator is not enabled, or has not yet completed its initial power-up sequencing.
- V_{DES} becomes higher than A_{VDD} - 1.0V.
- The output voltage exceeds the OVP and PWRGD tolerance limit.

The STAT pin is also driven LOW (and regulation stops) when one or more of the following conditions exists:

- There is an open or short (to ground) on the BIAS and I_{RIPL} pins.
- The die temperature has exceeded a threshold of approximately 150°C.
- There is a FUVLO/FOVLO/AUVLO fault condition.

None of the above conditions are latching. In all cases, once the fault condition is removed, regulation will resume. When OE is LOW, the entire IC is powered down. Therefore, the STAT pin is floating. Once OE goes HIGH, it is necessary to wait 600µS before reading the STAT pin to allow the IC's internal LDOs to power up. After 600µS, the STAT pin will be actively pulled LOW and then STAT will go HIGH once the regulator is operating normally, as defined above.

APPLICATIONS INFORMATION

Setting the Output Voltage

The desired output voltage is set on the V_{DES} pin according to Equation 7:

Equation 7

$$V_{DES} = V_{DES0} \bullet \left(\frac{R_{DES} + R_F}{48.7k\Omega}\right)$$

Table 1: R_{DES} For Typical Output Voltages

V_{OUT} (V)	0.7	1.05	1.2	1.8	2.5	3.3	5.0
R_{DES} (kΩ)	27.7	41.7	47.5	71.5	71.5	71.5	71.5
R_{FB1}(Ω)	–	–	–	–	69.8	92	138
R_{FB2}(Ω)	–	–	–	–	178	110	77.7

The following restrictions should be observed

- V_{DES} should be no lower than 0.7V
- V_{DES} should not be greater than 1.8V

If an output voltage higher than 1.8V is required a voltage divider on V_{OUT} should be used to constrain the voltage on V_{SENSE}+ and keep V_{DES} within the 1.8V limit.

For example, to set V_{OUT} = 2.5V, a feedback divider can be used in order to keep V_{DES} at 1.8V. Specifically, R_{DES} is chosen according to Equation 8 in order to program V_{DES} not to exceed 1.8V (see example in Table 1).

Equation 8

$$R_{DES} = 48.7k\Omega\left(\frac{V_{DES}}{V_{DES0}}\right) - R_F$$

With a V_{DES} voltage of 1.8V, a gain boost of 1.39x is required to set V_{OUT} to 2.50V. The gain boost is described by Equation 9:

Equation 9

$$A_V = 1 + \frac{R_{FB1}}{R_{FB2}}$$

From this equation, it can be seen that a selection of $R_{FB1} = 0.39 \bullet R_{FB2}$ will yield a gain of 1.39x. The total parallel resistance of $R_{FB1} || R_{FB2}$ should be constrained to 50Ω. The unique solution of both R_{FB1} and R_{FB2} to satisfy both constraints is R_{FB1} = 69.8Ω and R_{FB2} = 178Ω.

Figure 7 shows this circuit.

Operation

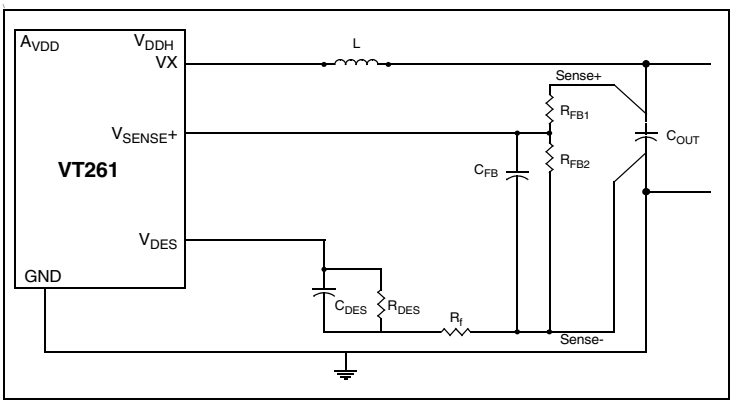


Figure 7: Configuration with Feedback Divider
V_{OUT} > 1.8V

Output Voltage Accuracy

The desired output voltage (V_{DES}) is set using resistors R_{BIAS} = 48.7kΩ and R_{DES} according to Equation 10. The error amplifier contributes an additional offset to V_{OUT}. Thus, the tolerances of V_{DES0}, R_{DES}, R_{BIAS} and V_{IN-OS} all affect the DC output voltage accuracy in accordance with Equation 10.

Equation 10

$$V_{DES} = V_{DES0} \bullet \left(\frac{R_{DES} + R_F}{R_{BIAS}}\right)$$

$$V_{OUT} = V_{DES} \pm V_{IN-OS}$$

where

- V_{DES0} has value and tolerance as defined in electrical characteristics table
- R_{DES}, R_F, and R_{BIAS} have manufacturer-specified resistance tolerances and temperature coefficients
- V_{IN-OS} is the error amplifier's input offset voltage as defined in Electrical Characteristics table

Maxim has partnered with two thin-film resistor manufacturers to create cost-effective 0.1% tolerance, ±25ppm/°C resistors in 0603 case sizes. The two values enabled are 41.2kΩ and 115kΩ, although other values are available upon request from these manufacturers. The part numbers and contact information for these two sources are listed in Table 2.

Table 2: Resistor Suppliers

Company	Value	Accuracy	Temperature Coefficient	Case Size	Part Number	Phone	Website
Thin-Film Technology	41.2kΩ 115kΩ	±0.1% ±0.1%	±25ppm/°C ±25ppm/°C	0603 0603	RR0816P4122B-T5 RR0816P1153B-T5	(507) 625-8445	www.thin-film.com
Venkel Ltd.	±1.0%	±0.1% ±0.1%	±25ppm/°C ±25ppm/°C	0603 0603	TFC0603-16W-E-4122BT TFC0603-16W-E-1153BT	(800) 950-8365	www.venkel.com

Output Voltage Ripple

Output voltage ripple is discussed in more detail in "Output Capacitor Selection." An approximation for the output voltage ripple is provided in Equation 11.

Equation 11

$$V_{PP} = ESR(I_{OUTRIPL}) + ESL\left(\frac{V_{IN}}{L}\right) + \left(\frac{I_{OUTRIPL}}{8fC_{OUT}}\right)$$

where

ESR = equivalent series resistance at the output capacitor
$I_{OUTRIPL}$ = peak-to-peak inductor current ripple
ESL = high-frequency equivalent series inductance at the output capacitor

Operation

Selecting the Error Amplifier Setting

The error amplifier has four gain settings (Ki) in order to accommodate a wide range of C_{OUT} configurations and maintain stability. The settings are selected by R_SEL according to Table 3.

Table 3: R_SEL Programming

R_{SEL} (Ω) (5%)	I_{MAX} (A)	AC Droop (mV)[1]	Ki	Min C_{OUT}[2] (µF)
GND	20	30	400000	300
11K	20	90	133000	150
22K	13.3	30	267000	200
91K	13.3	20	400000	300

Note 1: AC droop with full I_{MAX} step and no feedback divider. With feedback divider, AC droop scales by A_V.

2: For improved transient and ripple performance, use minimum C_{OUT} x1.5 or more.

The R_SEL resistor value is determined internally in the first 300µsec at startup. Once R_SEL has been determined, the pin voltage returns to zero.

Which setting to use is determined as follows:

1. Select C_{OUT} based on output voltage ripple requirements (see Equation 11).
2. Calculate unloading transient performance - add C_{OUT} if improvement required, as shown in Equation 12.

Equation 12

$$UnloadingTransient(v) = \frac{L_{OUT} \bullet \left(I_{MAXLOADSTEP} + \frac{I_{OUTRIPL}}{2}\right)^2}{2 \bullet C_{OUT} \bullet V_{OUT}}$$

3. The loading transient seen on V_{OUT} for a full-load step is determined by the error amplifier setting as shown in Table 3. For smaller load steps, the transient is proportionately smaller. With a voltage divider in the feedback, the transient is larger by a factor of 1 over the divide ratio. Choose the closest (but lower) Error Amplifier Setting to meet your transient requirement.
4. Choose the highest C_{OUT} based on steps 1-3.

The C_{OUT} chosen must also satisfy the minimum requirements described in the stability section.

Stability/Compensation

There are no elaborate compensation networks required unlike voltage mode controllers which require networks in order to stabilize the feedback loop. The VT261 has a minimum C_{OUT} requirement which is sufficient to meet all stability requirements (as shown in Table 3).

Thermal Considerations

The power dissipation curves can be used in conjunction with the Junction temperature vs Power dissipation curve to match the appropriate thermal system to keep the junction temperature within a specified value. The Safe Operating Area (SOA) chart has been developed to show the maximum usable current at any output voltage for a given thermal environment. The SOA is based on a junction temperature of 125°C.

External Components Selection

EXTERNAL COMPONENTS SELECTION

Table 4 provides a comprehensive list of external components required to complete the regulation system shown in Figure 8. More detailed information on component selection for the output filter is provided in the following sections.

Table 4: Recommended External Components

Component	Schematic Reference	Value	Quantity	Comments
Input Capacitor	C10, C11	10µF, 22µF	1 each	X5R or X7R 16V or 25V
Input HF Bypass Capacitor	C8	0.1µF	1	X5R 0603 size
Input HF Bypass Capacitor	C9	1.0µF	1	X5R 0603 size
A_{VDD} Bypass Capacitor	C12	0.47µF		X5R 0603 size
EN Bypass Capacitor	C5		1	X5R 0402 size
C_{DES} Capacitor	C6		1	X5R 0402 size
Output Capacitors	C_{OUT}	See Table 3 and Table 6	See Table 3 and Table 6	X5R or X7R 6.3V Low Profile
R_{BIAS} Resistor	R2	48.7kΩ, 0.5%	1	0402 size
R_{DES} Resistor	R5	See Table 1, 0.5%	1	0402 size
Output Inductor	L1	210nH	1	
Output HF Bypass Capacitor	C2	0.1µF	1	X5R, 0402 size
Output HF Bypass Capacitor	C1	6.8nF	1	X5R, 0402 size

Inductor Selection

The output inductor has an important influence on the overall size, cost and efficiency of the voltage regulator. Smaller inductor values usually correspond to larger saturation current ratings, smaller physical sizes or both. Since the inductor is typically one of the larger components in the system, a minimum inductor value is particularly important in space-constrained applications. Smaller inductor values also permit faster transient response. For any buck regulator, the maximum current slew rate through the output inductor is given by Equation 13.

Equation 13

$$SlewRate = \frac{dI_L}{dt} = \frac{V_L}{L}$$

where

I_L = *inductor current*
L = *output inductance*
V_L = *voltage drop across the inductor*

This equation implies that larger inductor values limit the regulator's ability to slew current through the output inductor in response to step load transients. Consequently, more output capacitors are required to supply (or store) sufficient charge to maintain regulation while the inductor current "catches up" to the load. In contrast, smaller inductor values increase the regulator's maximum achievable slew rate and decrease the necessary capacitance, at the expense of higher ripple current. The peak-to-peak inductor ripple current is given by Equation 14 and should be 25% to 50% of the IC's rated current.

Equation 14

$$I_{OUTRIPL} = \frac{V_{OUT} \bullet (V_{IN} - V_{OUT})}{V_{IN} \bullet L_{OUT} \bullet Fsw}$$

where

Fsw = *switching frequency*
L_{OUT} = *output inductor value*
V_{IN} = *input voltage*
V_{OUT} = *output voltage*

From this equation it is clear that for the same switching frequency, ripple current increases inversely as L_{OUT} decreases. This increased ripple current results in increased AC loss, larger peak current and, for the same output capacitance, results in increased output voltage ripple. The saturation current rating of the inductor is another important consideration. In periodic steady state at full load, the peak inductor current is given by Equation 15.

Equation 15

$$I_{PK} = I_{MAX} + \frac{I_{OUTRIPL}}{2}$$

where

I_{MAX} = *maximum DC load current*
$I_{OUTRIPL}$ = *peak-to-peak inductor current ripple (defined above)*

For proper operation of the regulator, it is important that I_{PK} never exceeds the saturation current rating of the inductor (I_{SAT}) during steady-state operation. It is recommended that a margin of at least 20% is included between I_{PK} and I_{SAT}, shown in Equation 16.

External Components Selection

Equation 16

$$I_{SAT} > 1.2 \bullet I_{PK}$$

Finally, the power dissipation of the inductor influences the regulation efficiency. Losses in the inductor include core loss, DC resistance loss and AC resistance loss. For best efficiency, use inductors with ferrite core material exhibiting low loss in the range of 0.5MHz to 2MHz and low DC winding resistance.

Table 5 provides a summary of recommended inductor suppliers.

Table 5: Inductor Suppliers

Company	Phone	Website
Cooper Electronics	(561) 752-5000	www.cooperet.com
Pulse	(858) 674-8159	www.pulseeng.com
Vishay-Dale	(605) 665-9301	www.vishay.com
Vitec	(760) 918-8831	www.viteccorp.com
Wurth	(201) 785-8800	www.we-online.com

Output Capacitor Selection

Output capacitance is selected to provide suitable transient tolerance and output voltage ripple. For the best performance, lowest cost and smallest size, Multilayer Ceramic Chip (MLCC) capacitors with 1210 or smaller case sizes, capacitance values of 22µF or smaller, 6.3V voltage ratings and X5R or better temperature characteristics are recommended. In VT261 systems with large transient load steps and MLCC output capacitors, it is generally the value of capacitance rather than the series parasitics of those capacitors that determines the transient tolerance. If desired, more capacitance can be added at the output to tighten transient tolerance at the expense of increased size, cost and component count. For a given load step magnitude ΔI_{LOAD}, output inductor value L, peak-to-peak ripple current $I_{OUTRIPL}$, input voltage V_{IN} and output voltage V_{OUT}, the transient overshoot and undershoot generally scale inversely with the value of output capacitance (C_{OUT}). For larger load steps with the same tolerance, capacitance should be increased with load step magnitude and peak-to-peak ripple current according to Equation 17.

Equation 17

$$C_{OUT} \propto \left(\Delta I_{LOAD} + \frac{I_{OUTRIPL}}{2}\right)^2$$

The voltage undershoot associated with a loading transient generally scales inversely with (V_{IN} - V_{OUT}). Similarly, the voltage overshoot associated with an unloading transient scales inversely with V_{OUT}. For the same transient tolerance, C_{OUT} generally scales linearly with L.

The transient tolerance of VT261 systems is ultimately limited by the infinite high-frequency transconductance of the integrated error amplifier. The Error Amplifier Operation section of this data sheet provides a description of the phenomenon and a closed form expression to predict the minimum achievable transient undershoot and overshoot. This transient tolerance improves linearly with decreasing load step magnitude and increasing Ki.

Output voltage ripple is another important consideration in the selection of output capacitors. For a buck regulator operating in Continuous Conduction Mode, the total voltage ripple across the output capacitor bank can be approximated as the sum of three voltage waveforms: 1) the triangle wave that results from multiplying the AC ripple current by the ESR, 2) the square wave that results from multiplying the ripple current slew rate by the ESL and 3) the piecewise quadratic waveform that results from charging and discharging the output capacitor. Although the phasing of these three components does impact the total output ripple, a common approximation is to ignore the phasing and to find the upper bound of the peak-to-peak inductor ripple by summing all three components, as shown in Equation 18.

External Components Selection

Equation 18

$$V_{PP} = ESR(I_{OUTRIPL}) + ESL\left(\frac{V_{IN}}{L_{OUT}}\right) + \left(\frac{I_{OUTRIPL}}{8FswC_{OUT}}\right)$$

where

- ESR = *equivalent series resistance at the output*
- $I_{OUTRIPL}$ = *peak-to-peak inductor current ripple*
- ESL = *high-frequency equivalent series inductance at the output*
- V_{IN} = *input voltage*
- L_{OUT} = *output inductance*
- Fsw = *switching frequency*
- C_{OUT} = *output capacitance*

In a typical VT261 application with a bank of 1206 X5R 6.3V 10µF output capacitors, these three components are roughly equal. The ESL effect of an output capacitor on output voltage ripple cannot be estimated from the resonant frequency, but from the high-frequency (10MHz or above) impedance of that capacitor. The contribution to ESL of a single 1206 10µF output capacitor is between 0.2 and 0.3nH, rather than the 1.2nH usually quoted. PCB traces and vias in the V_{OUT}/GND loop contribute additional parasitic inductance. The final considerations in the selection of output capacitors are ripple current rating and power dissipation. Using a conservative design approach, the output capacitors should be designed to handle the maximum peak-to-peak AC ripple current experienced in the worst case. Because the recommended output capacitors have extremely low ESR values, they easily satisfy this ripple current requirement. For the triangular AC ripple current at the output, the total RMS current that needs to be handled is calculated, as shown in Equation 19:

Equation 19

$$I_{RMS_{COUT}} = \frac{I_{OUTRIPL}}{\sqrt{12}}$$

and the total power dissipation in the output capacitors is shown in Equation 20:

Equation 20

$$P_{COUT} = I^2_{RMS_{COUT}} \bullet ESR$$

where

- ESR = *equivalent series resistance of the entire output capacitor bank*

Table 6 provides a list of recommended output capacitors for the VT261 system. Each capacitor has a 1206 or smaller case size, a X5R or better temperature rating, a 6.3V or 4V voltage rating and a value of 22µF or smaller.

External Components Selection

Table 6: Capacitor Suppliers for MLCC Output Capacitors

Case Size	Value (µF)	Temperature Rating	Volt Rating	t[1]	Company	Part Number
1206	10	X5R	6.3V	1.6 0.85 1.6 1.6	AVX Murata Taiyo Yuden TDK	1206D106MAT2A GRM319R60J106KE19D JMK316BJ226ML C3216X5R0J106M
1206	10	X6S	4V 6.3V 4V	1.6	AVX Murata TDK	12064W106MAT2A GRM319C80J106KE19D C3216X6S0G106M
1206	22	X5R	6.3V	1.6	AVX Murata Taiyo Yuden TDK	12066D226MAT2A GRM31CR60J226KE19L JMK316BJ226ML C3216X5R0J226M
1206	22	X6S	4V	1.6	AVX Murata TDK	12064W226MAT2A GRM31CC80G226KE19L C3216X6S0G226M
1206	47	X5R	4V 6.3V	1.6	AVX Murata Taiyo Yuden TDK	12064D476MAT2A GRM31CR60J476ME19L JMK316BJ476ML C3216X5R0J476M
1206	47	X6S	4V	1.6	TDK	C3216X6S0G476M
0805	10	X5R	6.3V	1.25 1.25 0.85 1.25	AVX Murata Taiyo Yuden TDK	08056D106MAT2A GRM21BR60J106KE19L JMK212BJ106MD C2012X5R0J106M
0805	10	X6S	4V 6.3V 4V	1.6	AVX Murata TDK	08054W106MAT2A GRM21BC80J106KE19L C2012X6S0G106M
0805	22	X5R	6.3V	1.25 1.25 1.25 1.25	AVX Murata Taiyo Yuden TDK	08056D226MAT2A GRM21BR60J226ME39L JMK212BJ226MG C2012X5R0J226M
0805	22	X6S	4V 6.3V 4V	1.6	AVX Murata TDK	08054W226MAT2A GRM21BC80J226ME51L C2012X6S0G226M

Note 1: t indicates nominal thickness in mm.

External Components Selection

Input Capacitor Selection

The selection and placement of input capacitors are important considerations. High-frequency input capacitors serve to control switching noise. Bulk input capacitors are designed to absorb the pulsed DC current that is drawn by the regulator. For the best performance, lowest cost and smallest size of the VT261 system, MLCC capacitors with 1210 or smaller case sizes, capacitance values of 22µF or smaller, 18V voltage ratings and X5R or better temperature characteristics are recommended as bulk. The minimum recommended value of capacitance is 20µF (bulk) and 0.1µF (high-frequency) for the VT261 system. Because the bulk input capacitors must source the pulsed DC input current of the regulator, the power dissipation and ripple current rating for these capacitors are far more important than that for the output capacitors. The magnitude of the RMS input capacitor current can be approximated using Equation 21:

Equation 21

$$I_{RMS_{CIN}} = \frac{I_{LOAD}\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

where

I_{LOAD} = *output DC load current*

With an equivalent series resistance of the bulk input capacitor bank (ESR_{CIN}), the total power dissipation in the input capacitors is shown in Equation 22:

Equation 22

$$P_{CIN} = I^2_{RMS_{CIN}} \bullet ESR_{CIN}$$

For a VT261 system converting 12V to 1.5V with 5A of load current, the RMS current flowing through the input capacitor bank is equal to 1.85A. If one 10µF input capacitor in 1206 case is used, the overall bulk capacitance is 10µF and the overall ESR is 4mΩ. The power dissipation in the input capacitors is 11mW, yielding nearly 5°C in case temperature rise. For better performance and increased reliability, the number of bulk input capacitors should be increased to two or more. See Table 7 for a list of input capacitors.

The proximity of the input capacitors to the VT261 can have an important impact on efficiency and regulation. For optimum performance, the V_{DDH} rows should have 0.1µF high-frequency bypass and bulk input capacitance tied to the ground plane as close to the chip as possible. An uninterrupted ground plane should be used directly beneath the V_{DDH} traces which run from the input capacitors to the chip in order to minimize parasitic inductance. Table 7 provides a list of recommended bulk input capacitors for the VT261 system. Each capacitor has a 1210 or smaller case size, 125°C temperature rating and a 18V voltage rating.

Table 7: MLCC Input Capacitors

Case Size	Value (µF)	Temperature Rating	Voltage Rating	t[1]	Company	Part Number
0603	1	X7S X7R	16V	0.8[2]	Murata TDK	GRM188C71C105KA12D C1608X7R1C105K
0805	2.2	X7R	25V 16V 16V	1.25 1.25 1.25	Murata TDK AVX	GRM21BR71E225KA73L C2012X7R1C225M 0805YC225MAT
0805	4.7	X7R	16V	1.25	Murata	GRM21BR71C475K
1206	4.7	X7R	16V	1.65	AVX Murata	1206YC475MAT GRM31CR71C475KA01L
1206	10	X7R	16V	1.65	Murata TDK AVX	GRM31CR71C106KAC7L C3216X7R1C106M 1206YC106MAT
1210	10	X7R	16V 25V	2.0 2.5	Murata TDK	GRM32DR71C106KA01L C3225X7R1E106M
1210	22	X7R	16V	2.45 2.5 2.5	AVX Murata TDK	1210YC226MAT GRM32ER71A476K C3225X7R1C226M

Note 1: t indicates nominal thickness in mm.

2: Indicates capacitors with nominal thickness smaller than the minimum QFN package thickness.

External Components Selection

Printed Circuit Board Layout

PCB layout can dramatically affect the performance of the regulator. A poorly-designed board can degrade efficiency, noise performance and even control loop stability. At higher switching frequencies, layout issues are especially critical. As a general guideline, the input capacitors and the output inductor should be placed in close proximity to the regulator IC, while the output capacitors should be lumped together as close to the load as possible. Traces to these components should be kept as short and wide as possible to minimize parasitic inductance and resistance. Traces connecting the input capacitors and internal FETs on the IC require particular attention since they carry currents with the largest RMS values and fastest slew rates. The input capacitors should be placed as close to the input supply pins as possible. Preferably, there should be an uninterrupted ground plane located immediately underneath these high-frequency current paths, with the ground plane located no more than 8 mils below the top layer. By keeping the flow of this high-frequency AC current localized to a tight loop at the regulator, electromagnetic interference (EMI) can be minimized.

Voltage sense lines should be routed differentially directly from the load points. They should be routed in parallel and in close proximity to each other with common-mode filtering to the A_{GND} pin of the IC or a quiet section of the ground plane. The ground plane can be used as a shield for these or other sensitive signals to protect them from capacitive or magnetic coupling of high-frequency noise.

For remote-sense applications where the load and regulator IC are separated by a significant distance or impedance, it is important to place the majority of the output capacitors directly at the load. For system stability, all output capacitors should, ideally, be placed as close as possible to the load. In remote-sense applications, common-mode filtering is necessary to filter high-frequency noise in the SENSE lines.

The following layout recommendations should be used for optimal performance:

- Input bypass capacitors should be placed on the same PCB sides as the QFN, all referenced to a common ground plane directly beneath. Low-profile capacitors should be used to clear heatsink restrictions, so that capacitors are as close to the QFNs as possible.
- A low-impedance ground plane is essential in keeping all voltages referenced to a common ground.
- Multiple vias are recommended for all paths that carry high currents (i.e., GND, V_{DDH}, VX). Vias should be placed close to the chip to create the shortest possible current loops. Make sure via placement does not obstruct the flow of currents or mirror currents in the ground plane.
- The VX trace connecting the chip and output inductor should be kept short and wide to minimize resistive loss and should be shielded to a GND plane immediately beneath the trace to minimize noise coupling into surrounding circuits. The VX trace includes large and fast voltage transients greater than 12V amplitudes and dv/dt greater than 10V/ns.
- Because the VT261 utilizes its A_{GND} node for accurate reference and bias purposes, the GND and A_{GND} sections should be separated on the top layer of the PCB. A_{GND} should then be tied through a via to a quiet area of the ground plane in close proximity to the chip. Typically, the area directly next to the A_{GND} node is the most convenient spot.
- The capacitor that bypasses A_{VDD} should have its ground terminal tied directly to the ground plane with a single via, creating the shortest possible current loop between it and the chip.
- It is recommended that A_{GND} be treated as a separate signal and routed in as short a distance as possible to the resistors tied to the BIAS and I_{RIPL} outputs and to the common-mode filter capacitance on the SENSE lines. It is important that these A_{GND} lines do not connect to GND at any place other than at the A_{GND} ball.

Gerber files with layout information and complete reference designs can be obtained by contacting a Maxim account representative.

APPLICATION NOTES

Important application notes are available for this product. Maxim recommends that relevant application notes are reviewed prior to starting a design. Application notes for this product are available from the device-specific product page on Maxim's website at http://www.maximintegrated.com, or by contacting a Maxim account representative.

Reference Schematic

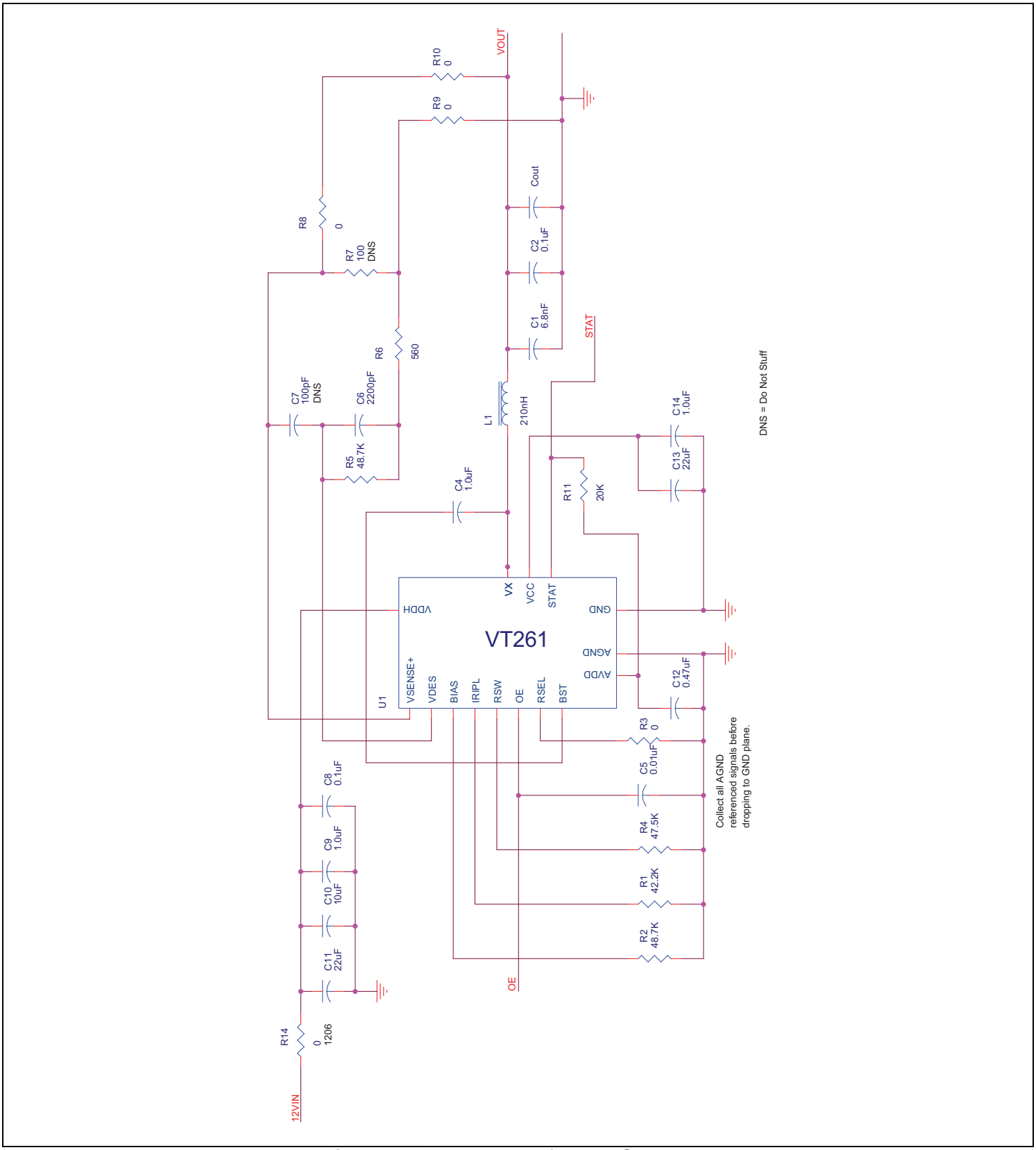


Figure 8: VT261 20A Reference Schematic

Packaging Information

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	Package Outline - 16 Lead QFN [Type C]	**ES AP-2104**	**0**
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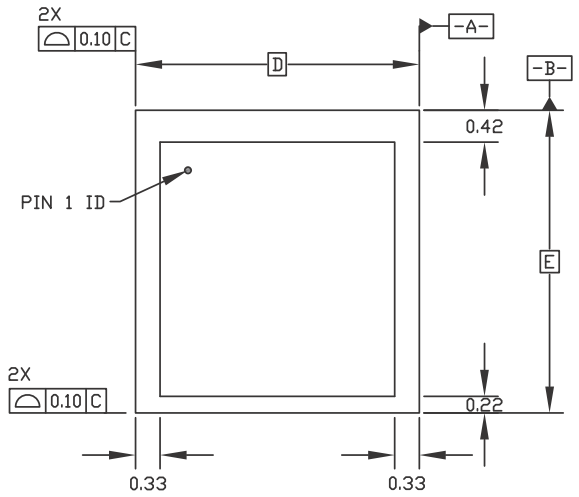
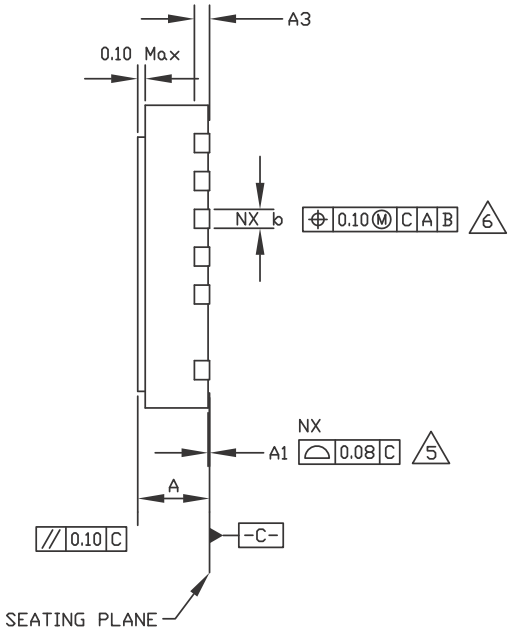
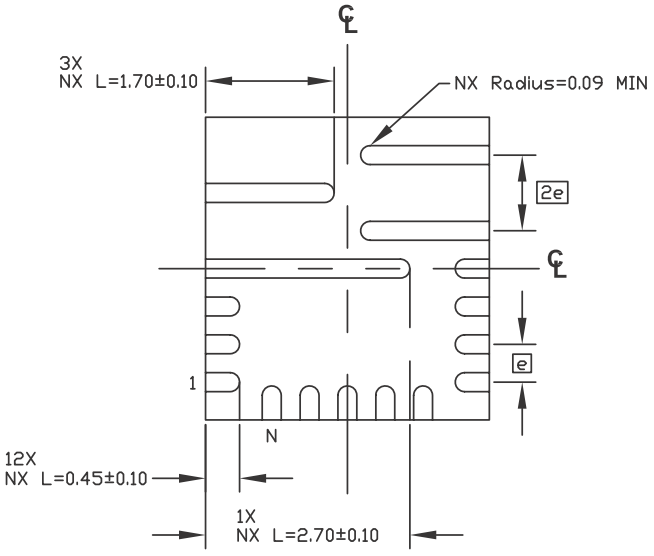
TOP VIEW



SIDE VIEW



BOTTOM VIEW



	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	0.95	1.00	0.035	0.037	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3		0.20 REF			0.008 REF	
b	0.18	0.25	0.30	0.007	0.010	0.012
D		3.75 BSC			0.148 BSC	
E		4.00 BSC			0.157 BSC	
e		0.50 BSC			0.020 BSC	
N		16 PINS			16 PINS	

NOTES:
1. Millimeters is the controlling dimension.
2. Drawing is not to scale.
3. N is the total number of terminals.
4. Dimensioning & tolerancing conform to ASME Y14.5M.-1994.
5. Coplanarity applies to the terminals and all other bottom surface metallization.
6. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measured in that radius area.

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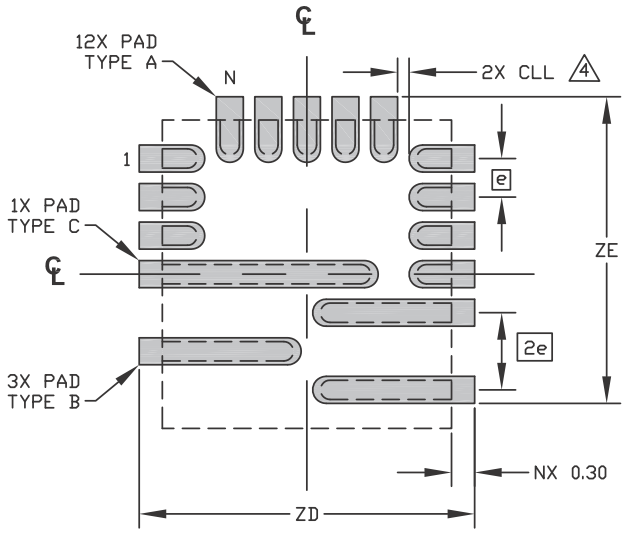
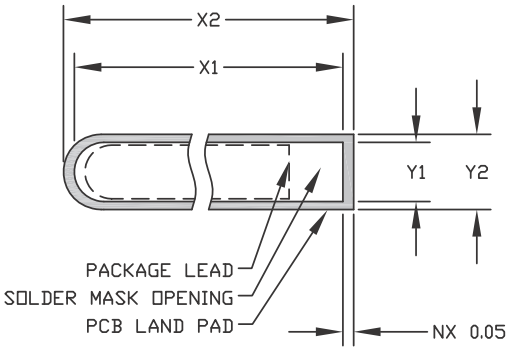
RECOMMENDED LAND PATTERN WITH PACKAGE OVERLAY



	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
CLL		0.15 REF			0.006 REF	
e		0.50 BSC			0.020 BSC	
N		16 PINS			16 PINS	
ZD		4.35 REF			0.171 REF	
ZE		3.98 REF			0.157 REF	

PAD DETAIL INFORMATION



	MILLIMETERS			INCHES		
DIM	TYPE A	TYPE B	TYPE C	TYPE A	TYPE B	TYPE C
Y1	0.28	0.28	0.28	0.011	0.011	0.011
Y2	0.35	0.35	0.35	0.014	0.014	0.014
X1	0.75	2.00	3.00	0.030	0.079	0.118
X2	0.85	2.10	3.10	0.033	0.083	0.122

NOTES:
1. Millimeters is the controlling dimension.
2. Drawing is not to scale.
3. N is the total number of terminals.
4. CLL is the corner pad edge to adjacent inside pad distance.

Revision History, Definitions, Disclaimers and Sales Contacts

VT261 REVISION HISTORY

Revision	Description	Date
0	Initial Data Sheet	N/A
1	Updated OCP Numbers in Electrical Characteristics Table Added PWRGD Min and Max Limits Expanded Regulator Status Section. Updated OE Pin Section and Voltage Regulator Enable Sections. Removed Specific Inductor Recommendations.	10/21/11
2	Changed “Overcurrent” to “Overvoltage” in OVP Section of Electrical Characteristics Table.	02/02/12
3	Updated Ordering Information Page Rebranded to Maxim Added Absolute Maximum Rating Information	01/09/14

Revision History, Definitions, Disclaimers and Sales Contacts

DATA SHEET PHASE DEFINITIONS

PRODUCT PREVIEW: Specifications are to be used as design targets for planning purposes as product is still in development stage.

PRELIMINARY: Specifications are based on limited product and system characterization as product is sampling and has not completed qualification.

NEW PRODUCT: Specifications are based on product and system characterization over all operating conditions as product has passed qualification and released to production.

FINAL: Specifications are based on volume manufacturing data and extensive field data as product has been in production over a year.

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